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| 09/597,523 | 06/20/2000 | Harry J. Beatty III | FIS9-1999-0317-US1 | 5256 |

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| EXAMINER | |
|---|---|
| PATEL, ASHOKKUMAR B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2127 | 5 |

DATE MAILED: 10/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/597,523 | Applicant(s) BEATTY III ET AL. | |
|---|---|---|---|
| | Examiner Ashok B. Patel | Art Unit 2127 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 June 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

**1.** Application Number 09/597523 was filed on 06/20/2000. Claims 1-18 are subject to examination.

### *Drawings*

**2.** The drawings are objected to because the Description of Related Art describes the reference characters 20b, 21b, 23b, 22b, 24b, program A, and program B in Fig.1. See page 1, lines 14-25. These reference characters are not present in Fig.1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Specification*

**3.** The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Parallel Processing by Creating Memory Hierarchal Levels".

**4.** The disclosure is objected to because of the following informalities: Related arts are lacking their corresponding serial numbers. See page1, lines 1-6. Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

**5.** 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

**6.** Claims 1-8 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. These claims recite computer memory structure, failing to recite any hardware necessary to render the claims tangible.

### *Claim Rejections - 35 USC § 112*

**7.** The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**8.** Claims 15-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear what Applicant's intended metes and bounds for claims 15-18 are. As written, it is believed these claims positively recite program instructions on a computer readable medium which cause parallel processing. The intended use is that of a computer memory structure having particular details set forth by Applicant; however, it is not seen how any of these details materially affect the "program storage device" or "program instructions" thereon. As such, it is believed the actual metes and bounds, as written, are significantly broader than Applicant intended. Rejections over prior art based on both what it is believed Applicant intended as the metes and bounds and what it is believed are the actual metes and bounds, as written, are recited below.

### *Claim Rejections - 35 USC § 102*

**9.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**10.** For the reasons stated above with respect to the § 112 rejection of claims 15-18, the following rejection is believed to apply.

Claims 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu (US 6,038,647).

Referring to claims 15-18, Shimizu teaches:

- A computer-readable medium encoded with a program for multi-access of a storage level including a plurality of pairs each comprising a data array and a tag array.., (col.32, lines 43-45).
- This multi-access method is applicable to a cache memory used in a high-performance parallel-processing architecture including a few processors having a common cluster., (Abstract).

Shimizu clearly shows a program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method for parallel processing using a computer memory structure.

### *Claim Rejections - 35 USC § 103*

**11.** The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**12.** Claims 1-4, 6-8, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meyer (6,397,299) in view of CAI et al. (hereinafter CAI) (Pub. No. US 2001/0049770 A1.).

Referring to claims 1-4 and 6-8, Meyer teaches "in a computer system, for configuring a memory subsystem, comprising selecting a subset of main memory, integrating the subset of main memory within the computer system such that the subset is physically distinct from the main memory and configuring the subset of main memory as non-cacheable memory. ", see Abstract. Meyer does not teach any contents of the memory or it's subset. CAI teaches, "**A buffer memory in the system has multiple buffer sections.** Each buffer section is **adapted to store information associated with requests from a corresponding one of the multiple execution entities**., page 1, paragraph [0008]. " For example, a **program execution entity**, such as a process, task, or **thread**, associated with a multimedia application may transfer large blocks of data (e.g., video data) that are typically not reused., page 1, paragraph [0005]. Each buffer section may be **a separate buffer module** or may be **a portion of a buffer memory that is separately addressable** (that is, memory is separated into different address

spaces)., page 1, paragraph [0017]." CAI also teaches, "The individual buffer sections may be **separately configurable** and may be assigned to store information of **different program execution entities in the system**.", page 1, paragraph [0017]. Thereby, CAI suggests that individual buffer sections are configurable regardless of other buffer sections in the buffer as well the buffer itself, as such any level in the hierarchy as well as the content within a given level of hierarchy is made separately configurable. The references of Meyer modified by CAI fail to teach to form another level of hierarchy. However, it is well known in the art to repeat a process, in this case, for example, adding another level of hierarchy, until the additions provide diminishing return over the objective of providing a parallel processing structure which reduces cost and errors in creating, managing, and terminating a thread. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to modify Meyer in order to accommodate CAI's "program execution entity", that is "thread", and made adapted to store information such as a heap, a stack and the variables. Also, when a buffer section (a first level of hierarchy, a plane) is made a portion of a buffer memory (a second level of hierarchy, a space) as suggested by CAI, it would have been also obvious to one having ordinary skill in the art at the time of invention was made to modify the buffer (a second level of hierarchy, a space) to contain common data accessible by all buffer sections (planes) of that buffer and add an additional level (third) of hierarchy containing "spaces", common data accessible by the spaces and, spaces and the third level of hierarchy containing the same or different program structures since each space and each level of hierarchy is separately configurable as suggested by CAI.

As a result, the hierarchy of memory is formed as a separate entity from systems main memory and cache as suggested by Meyer and the levels of hierarchy is formed such as a buffer (space) containing common data accessible by buffer sections (planes) and each buffer having a multiple buffer sections (planes) incorporating one program executing entity, thread, where each buffer section is adapted to store information such as a heap, a stack and the variables. Because the levels of hierarchy along with combinations of same or different program structures provide a parallel processing structure which is less subject to serialization limitations.

**13.** Claims 9 and 10 are claims to computer program comprising a computer usable medium having computer readable code embodied in the medium for a computer memory structure of claims 1 and 2. Therefore, claims 9 and 10 are rejected for the reasons set forth in above paragraph 12 for the claims 1-4 and 6-8.

**14.** Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art as applied to claim 1 above, and further in view of Arimilli et al. (hereinafter Arimilli) (US 6,473,833).

Referring to claim 5, keeping in mind what Meyer and CAI teach as indicated above, the references of Meyer modified by CAI fail to teach the function tables at various levels of storage (memory) hierarchy. Arimilli teaches: "Values within a level are indexed by a directory that provides an indexing of information relating the values in that level to the

next lower level. In a preferred embodiment of the invention, the directories for the various levels of storage are contained within the next higher level, providing a faster access to the directory information. Cache memories used as the highest levels of storage, and one or more sets are allocated out of that cache memory for containing a directory of the next lower level of storage. An address comparator which is used to compare entries in a directory to address values is directly coupled to the set or sets used for the directory, reducing the time needed to compare addresses in determining whether an address is present in the cache.", see Abstract. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to modify and enhance the levels of hierarchy such as "spaces" and the "third level" with Arimilli's directory (function Table) that provides an indexing of information relating to the values to locate the Value (data). Because indexing of information provides a parallel processing structure less subject to serialization limitations in accessing common system services such as data structures.

**15.** Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meyer (6,397,299) in view of CAI et al. (hereinafter CAI) (Pub. No. US 2001/0049770 A1.).

Referring to claim 11, keeping in mind the teachings of Meyer and CAI forming a hierarchy of memory structure as above, in addition CAI also teaches "To take advantage of the multitasking or multithreading capabilities of a system, the independent cache modules of a multi-unit cache memory may be assigned to store information of corresponding execution entities. Thus, for example, execution entities of

a multimedia application may be assigned to one cache module, while execution entities of other applications may be assigned to different cache modules of the multi-unit cache memory.", page 2, paragraph [0021]., and "In addition, execution entities of different applications may be assigned the same EID. Thus, for example, a first execution entity of a multimedia application may be assigned EID 1, while a second execution entity of the multimedia application may be assigned EID 2. In the same system, execution entities of a spreadsheet application having similar data usage characteristics as the second execution entity of the multimedia application may also be assigned EID 2.", page 2, paragraph [0022]. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to store information (data) for each level (plane) separately and made it accessible only by an execution entity (thread) pertaining to that level (plane) as well as providing common data between each levels (planes) accessible to execution entity (thread) of another plane where the execution entities will not have to interact with each other. Because, the threads of different applications are kept active at a time without inter-thread interaction in a parallel processing structure which is less subject to serialization limitations.

**16.** Claim 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art as applied to claim 1 above, and further in view of Arimilli et al. (hereinafter Arimilli) (US 6,473,833).

Referring to claims 12, 13 and 14, keeping in mind the teachings of Meyer and CAI forming a hierarchy of memory structure as above, " CAI also teaches "The individual buffer sections may be **separately configurable** and may be assigned to store information of **different program execution entities in the system**.", page 1, paragraph [0017]. The references of Meyer modified by CAI fail to teach the directories of various levels of storage (memory) hierarchy. Arimilli teaches: "Values within a level are indexed by a directory that provides an indexing of information relating the values in that level to the next lower level. In a preferred embodiment of the invention, the directories for the various levels of storage are contained within the next higher level, providing a faster access to the directory information. Cache memories used as the highest levels of storage, and one or more sets are allocated out of that cache memory for containing a directory of the next lower level of storage. An address comparator which is used to compare entries in a directory to address values is directly coupled to the set or sets used for the directory, reducing the time needed to compare addresses in determining whether an address is present in the cache.", see Abstract. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to configure the levels of hierarchy such as "spaces" and the "third level" with same or different program structures comprising of program libraries along with the common data between the planes and spaces with Arimilli's directory (function Table) that provides an indexing of information relating to the values to locate the Value (data) and make it accessible by the threads. Because indexing of information and providing common data at each level of hierarchy provides a parallel processing structure less

subject to serialization limitations in accessing common system services such as data structures.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (703) 305-2655. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William A Grant can be reached on (703) 308-1108. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

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October 28, 2003

WILLIAM GRANT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/30/03